



FIG 1

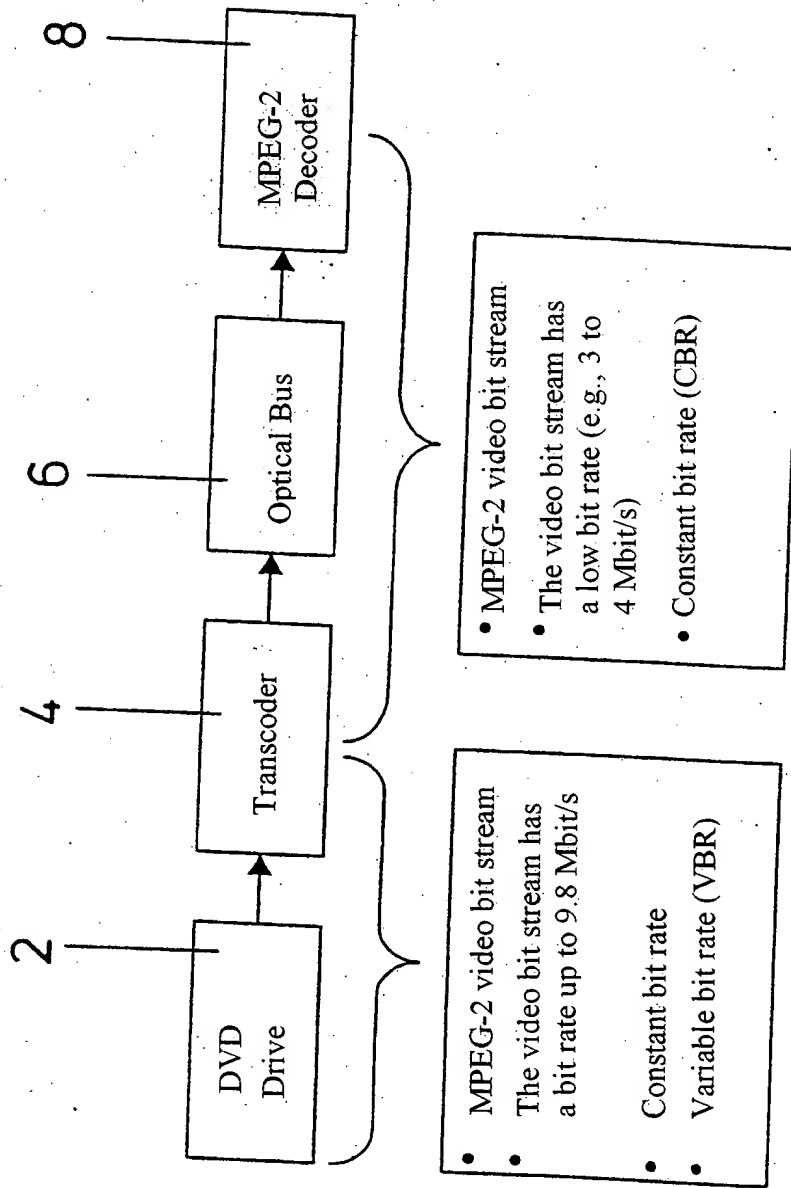


FIG 2

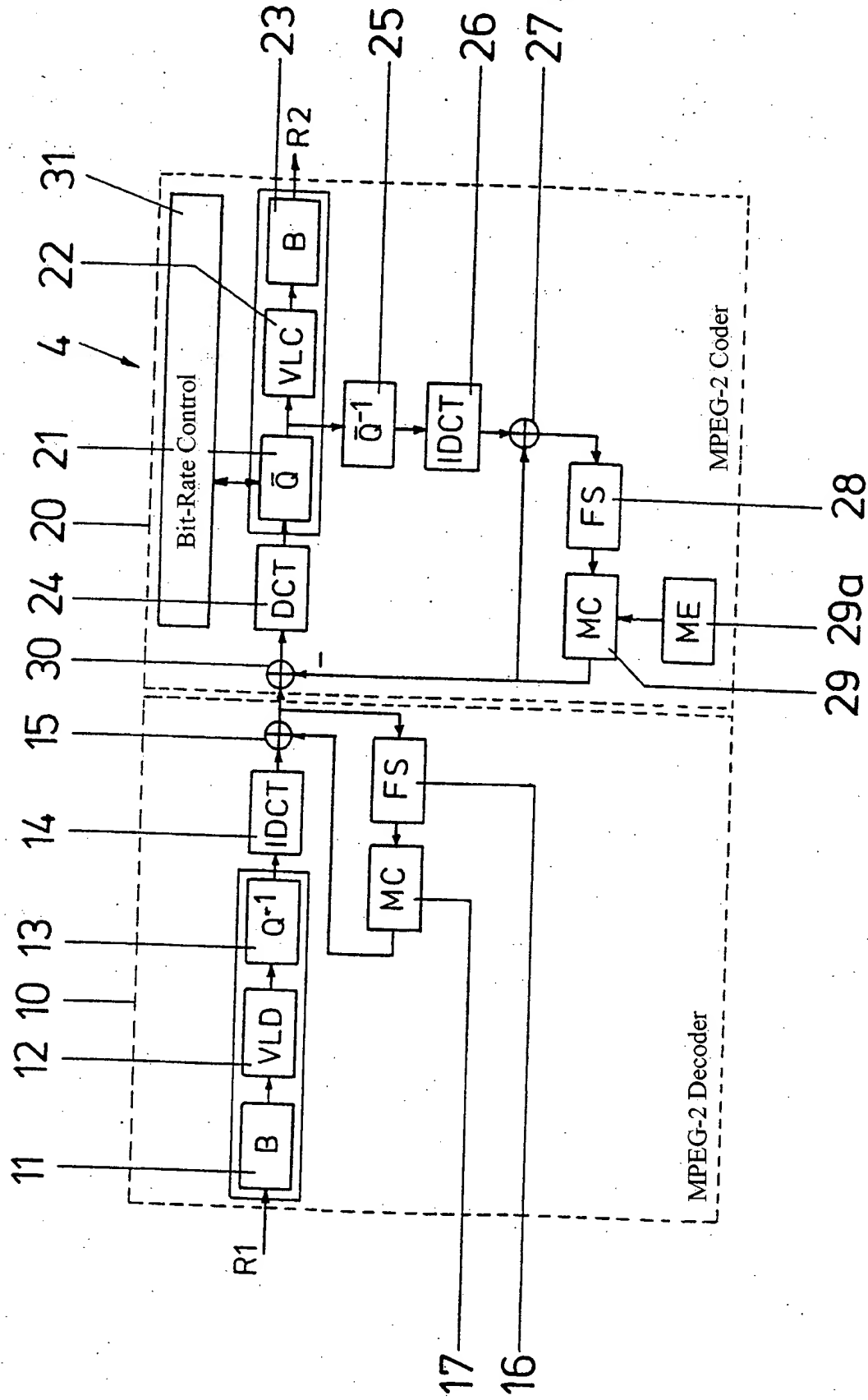
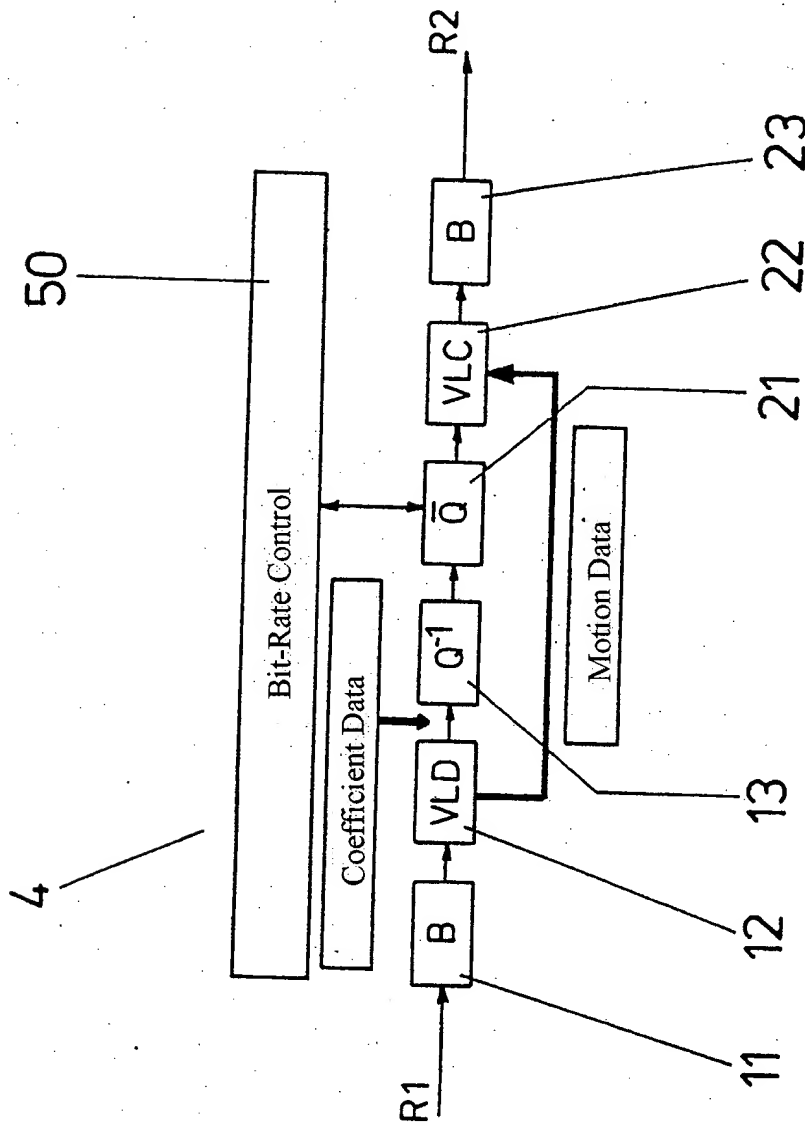


FIG 3



The diagram illustrates a computer system architecture with the following components and connections:

- Input (50):** An arrow pointing into the **ESTIMATION STAGE** (53).
- ESTIMATION STAGE (53):** The first processing stage, which outputs to the **VERIFICATION STAGE** (54) and the **BEST ALLOCATION STAGE** (56).
- VERIFICATION STAGE (54):** Receives input from the **ESTIMATION STAGE** and outputs to the **SEGMENT DETECTION STAGE** (55).
- SEGMENT DETECTION STAGE (55):** Outputs to the **BEST ALLOCATION STAGE** (56).
- BEST ALLOCATION STAGE (56):** Receives inputs from the **ESTIMATION STAGE** (53), **VERIFICATION STAGE** (54), and **SEGMENT DETECTION STAGE** (55). It outputs to the **ROUTE CONTROL STAGE** (52).
- ROUTE CONTROL STAGE (52):** Receives inputs from the **BEST ALLOCATION STAGE** (56), **SEGMENT DETECTION STAGE** (55), and external inputs **a**, **b**, **c**, **d**, **e**, **f**, **g**, and **h**. It outputs to the **ROUTING UNIT** (57).
- ROUTING UNIT (57):** Receives input from the **ROUTE CONTROL STAGE** (52) and outputs to the **MEMORY** (58).
- MEMORY (58):** The final destination for the data flow.

FIG 5

REPLACEMENT DRAWING SHEET

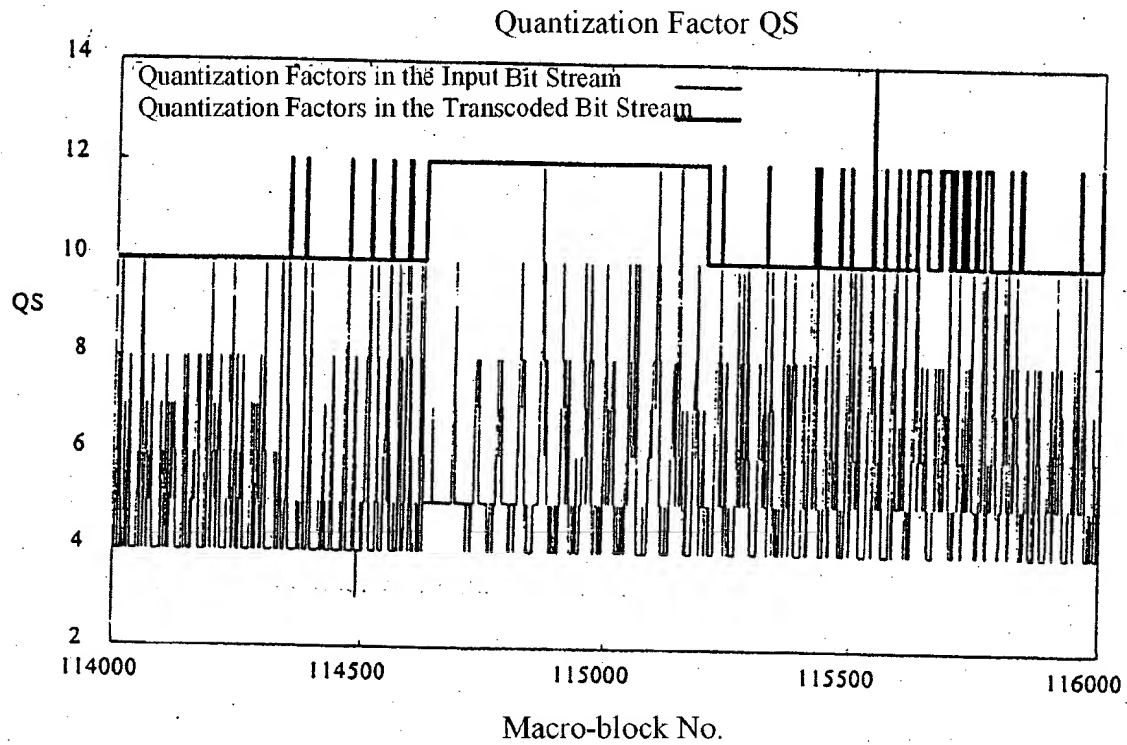


FIG 6

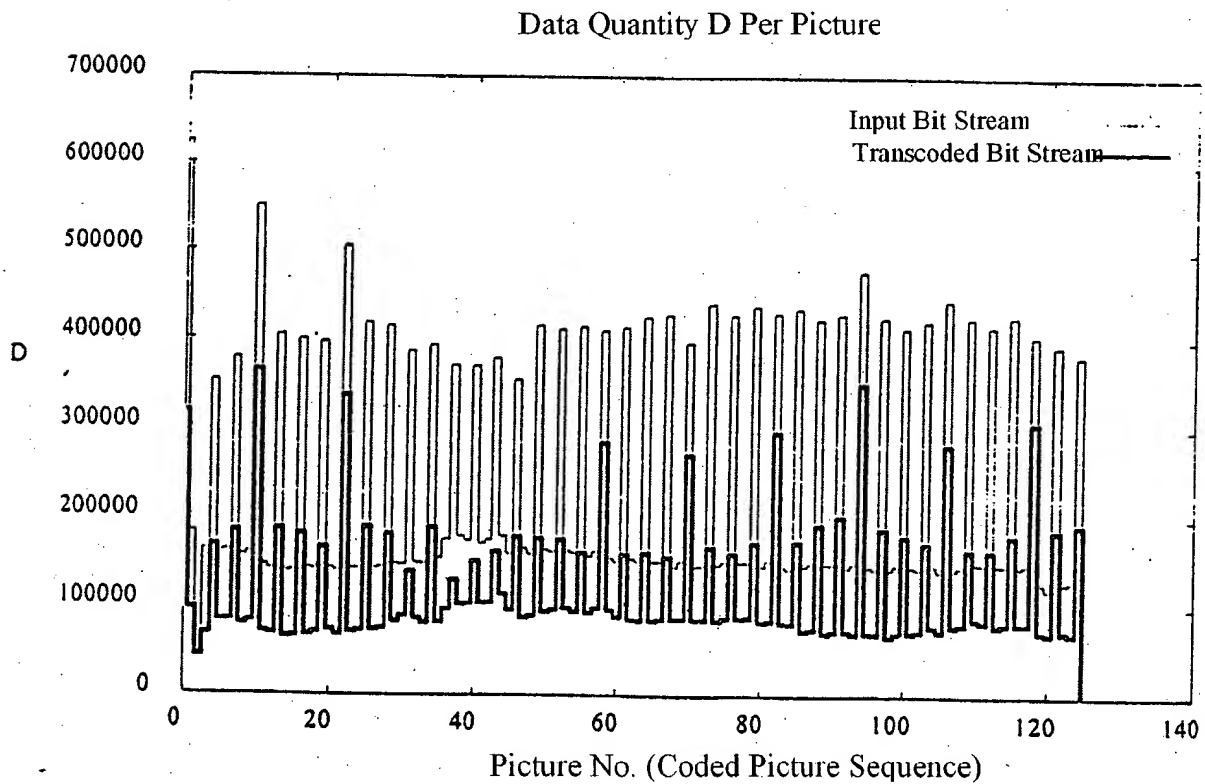


FIG 7

REPLACEMENT DRAWING SHEET

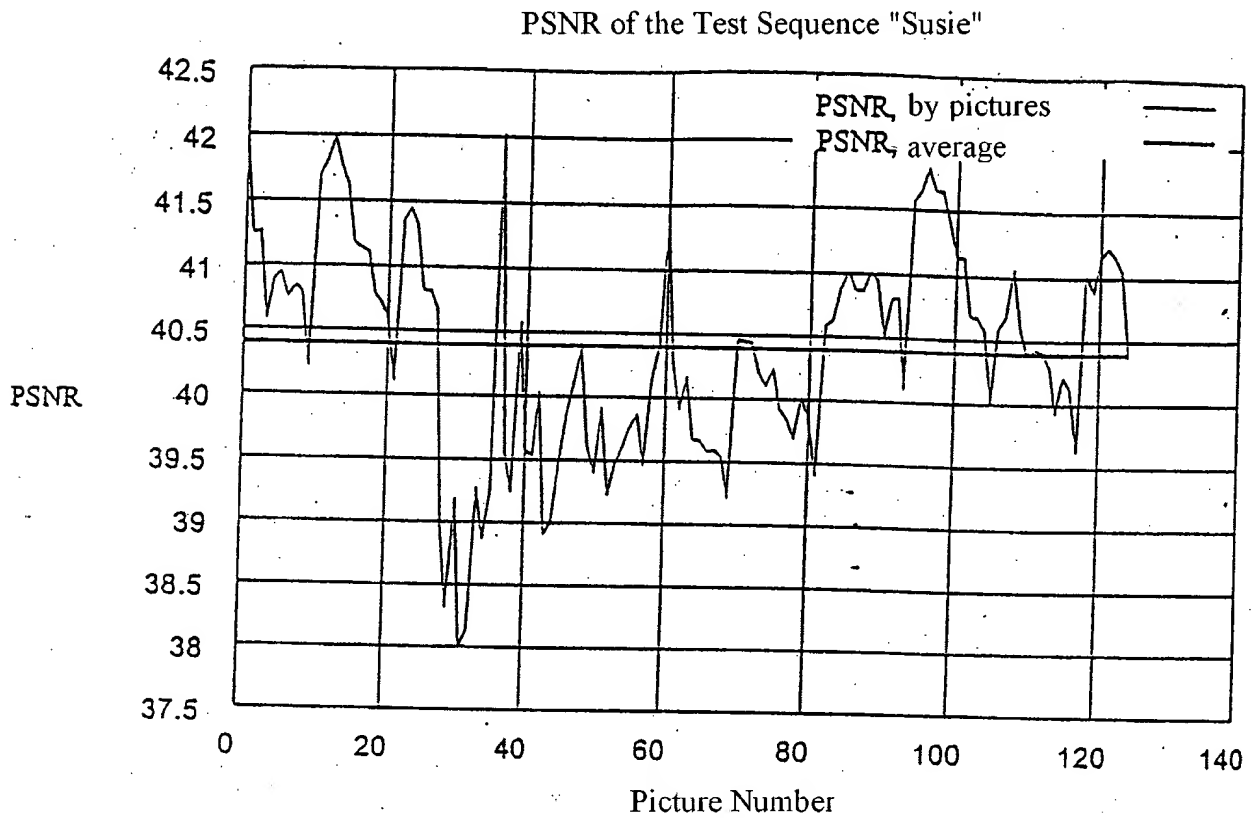
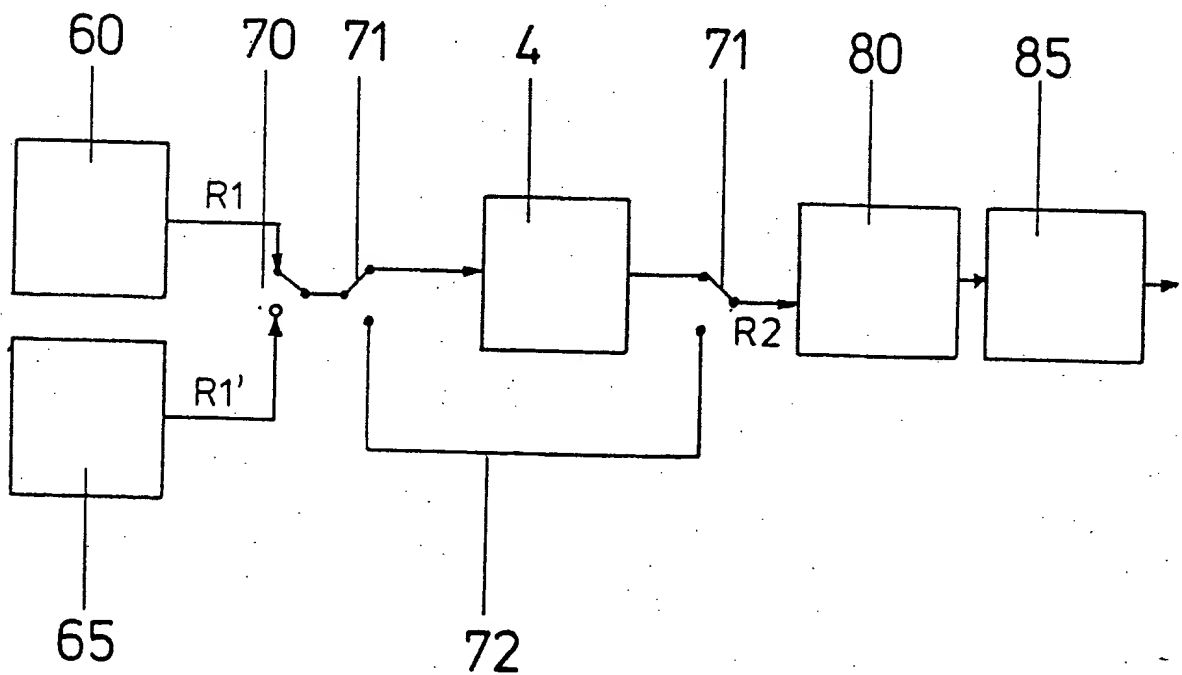


FIG 8



## REPLACEMENT DRAWING SHEET

FIG 9

